REMARKS

Claims 1 and 3 stand rejected under 35 U.S.C. § 102 as being anticipated by Andrews '737 ("Andrews"). Claim 1 is independent. This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "at least two logic circuits including a first logic circuit and a second logic circuit ***having the same function as said first logic circuit***; and a direction circuit for directing operation or halt of ***said first and second logic circuits***, wherein said direction circuit ... directs, in testing mode, ***simultaneous operation*** of said first and second logic circuits when said select signal is a signal for selecting said first ***or*** second logic circuit" (emphasis added).

Turning to Figure 7 of Andrews, the Examiner relies on CMOS Modules 1 and 2 as the claimed logic circuits and BICSC TDR 7 as the claimed direction circuit. However, the Examiner ***merely concludes*** that the CMOS Modules 1 and 2 have the same function, and that BICSC TDR 7 directs the operation of the CMOS Modules so as to enable, in testing mode, ***simultaneous operation*** of the CMOS Modules when the select signal is a signal for selecting the CMOS Module 1 ***or*** the CMOS Module 2. However, the Examiner does not identify precisely where Andrews allegedly discloses such features. In imposing a rejection under 35 U.S.C. §102, the Examiner is required to point to "page and line" wherein an applied reference is perceived to identically disclose each feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).

In fact, it is respectfully submitted that Andrews appears to be completely silent as to the two CMOS Modules having the same function. It is noted that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999).

Indeed, as described throughout Applicants' specification, one of the capabilities of the present invention is to detect a ***difference*** between the outputs of the respective logic circuits having the ***same*** function in order to identify any potential defects (*see, e.g.,* page 11, lines 1-21 of Applicants' specification). In this regard, the present invention does not need a current monitor.

Further, it is respectfully submitted that the BICSC TDR 7 of Andrews does NOT appear to direct the operation of the CMOS Modules, let alone in the particular manner recited in claim 1 in that ***simultaneous operation*** of the alleged logic circuits can be performed in response to a signal for selecting the first ***or*** second logic circuit. In contrast, as shown in Figure 7 of Andrews and described in the corresponding disclosure therein, the BICSC TDR 7 is connected to and operates the current monitors BIC 1 and 2 rather than operating the CMOS Modules.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Andrews does not anticipate claim 1, nor any claim dependent thereon.

Claims 2 and 4 stand rejected under 35 U.S.C. § 103 as being unpatentable over Andrews. Claim 4 is independent. This rejection is respectfully traversed for at least reasons similar to those discussed above with respect to claim 1 regarding the first and second logic circuits having the same function.

Claim 4 recites in pertinent part, "simultaneously operating said first and second logic circuits ... ." Again, the Examiner merely concludes that the CMOS Modules 1 and 2 are

simultaneously operated, but there does not appear to be any disclosure that ***necessitates*** that they are in fact simultaneously operated. It is again noted that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999).

Claim 4 further recites in pertinent part, "transferring outputs of said ***first and second logic circuits*** to one signal line." The Examiner alleges that Andrews discloses "transferring the outputs of the (BIC 1 and 2) current monitor to a signal line ... ." The relevance of this allegation to the aforementioned feature recited in claim 4 is not understood. That is, claim 4 refers to the outputs of the alleged logic circuits CMOS Modules 1 and 2, and not to the outputs of the current monitors BIC 1 and 2. As understood in the art, the outputs of the current monitors BIC 1 and 2 can not be interpreted as the outputs of the CMOS Modules 1 and 2. Indeed, as expressly relied on by the Examiner with respect to claim 2, the Examiner has interpreted the current monitors as the claimed first and second output circuits *for receiving the outputs from the first and second logic circuits*, respectively.

Moreover, as shown in Figure 1 of Andrews, the output of a CMOS Module is input into a comparator VCOMP of the current monitor so as to be compared with a reference voltage VREF. Based on this comparison, a fault signal is output from the current monitor. It is this fault signal that is output to the BICFCP TDR6, NOT the output of the CMOS Module. As mentioned above, the present invention does not need a current monitor because it can enable the capability to detect fault based on a difference between the outputs of the same-function logic circuits (without needing to compare each output with a VREF) (*see, e.g.*, page 11, lines 1-21 of Applicants' specification).

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 4 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1 and 4 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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